

## **Chapter 4**

## **FPGA Hardware Implementation**

## 4.1 Code Editing Input and System Compilation

### 4.1.1 Design File Edit and Input

New Outsthus II Designt	·····································	保存在(I):	MY_PROJECT	- +	<b>€</b> 💣 III 🔻
<ul> <li>New Quartus II Project</li> <li>Design Files         <ul> <li>AHDL File</li> <li>Block Diagram/Schematic File</li> <li>EDIF File</li> <li>Qsys System File</li> <li>State Machine File</li> <li>SystemVerilog HDL File</li> <li>Td Script File</li> <li>Verilog HDL File</li> <li>VHDL File</li> </ul> </li> <li>Memory Files         <ul> <li>Hexadecimal (Intel-Format) File</li> <li>Memory Initialization File</li> </ul> </li> <li>Verification/Debugging Files         <ul> <li>In-System Sources and Probes File</li> <li>Logic Analyzer Interface File</li> <li>SignalTap II Logic Analyzer File</li> </ul> </li> </ul>	<pre>1 module CNT10 (CLK,RST,E 2 input CLK,EN,RST,LO 3 input [3:0] DATA; 4 output [3:0] DOUT; 5 output COUT; 6 reg [3:0] Q1; 7 assign DOUT = Q1; 8 always @(posedge CI 9   begin 10    if (!RST 11   else if (EN) be 12    if (!LOA 13    else if (Q1) 14    else Q1 &lt;= 15    end 16    always @(Q1) 17    if (Q1==4'h9) CO 18    endmodule 19    !</pre>	<ul> <li>最近访问的位置</li> <li>桌面</li> <li>菜面</li> <li>菜面</li></ul>	名称 □ CNT10.v CNT10.v 文件名(N): CNT10.v 保存类型(T): Vvvi10.v	۳. ۱۳.	修改日期 2017/5/6 21:07

Figure: Select edit file type

Figure: Edit input source program and save it

Any EDA design is a project, and you must firstly create a folder for this project that holds all the design files associated with the project. Different design projects are best placed in different folders, and all files for the same project are in the same folder.

## 4.1 Code Editing Input and System Compilation

### 4.1.2 Creating a Project

	💱 New Project Wizard	<u> </u>
	Directory, Name, Top-Level Entity [page 1 of 5]	
	What is the working directory for this project?	
	D:\MY_PROJECT	
	What is the name of this project?	
	CNT10	
Fine-pitch Ball Grid Array	What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.	
1 2	CNT 10	
	Use Existing Project Settings	

### Figure: Creating project CNT10 using New Project Wizard

Family & D Select the family a You can install add	Device Settin and device you want ditional device suppor	<b>gs [pa</b> to target fi rt with the	ge 3 of 5] or compilation. Install Devices cor	nmand on th	ne Tools menu.				EDA Tool Se Specify the other El	e <mark>ttin</mark> DA tool
Device family					Show in 'Ava	ilable devices' list			EDA tools:	
Device family					SHOW IT AVA				Tool Type	1
Family: Cyclon	ne IV E			•	Package:	FBGA		•	Design Entry/Synth	nesis
Devices: All				¥.	Pin count:	484		•	Simulation	Ĩ
Target device					Speed grade	: 8		•	Formal Verification	Ĩ
Target device					Name filter:				Board-Level	
O Auto device	selected by the Fitte	er								5
Specific dev	rice selected in 'Availa	able device	s' list		Show ad	vanced devices				5
Other: n/a										E
Available devices:										
Name	Core Voltage	LEs	User I/Os	Memo	ory Bits	Embedded multiplier 9-bit elements	PLL	ial Ck	🛛 🛛 Figui	re:
EP4CE15F23C8	1.2V	15408	344	516096	112	2	4	20		
EP4CE30F23C8	1.2V	28848	329	608256	13	2	4	20		
EP4CE40F23C8	1.2V	39600	329	1161216	23	2	4	20		

EDA Tool Setti	ngs [page 4 o	of 5]			
Specify the other EDA to	ols used with the Qua	rtus II s	oftware to develo	p your pr	oject.
EDA tools:					
Tool Type	Tool Name		Format(s)		Run Tool Automatically
Design Entry/Synthesis	<none></none>	•	<none></none>	Ŧ	Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	-	Verilog HDL	•	Run gate-level simulation automatically after compilation
Formal Verification	<none></none>	•			
Board-Level	Timing		<none></none>	•	
	Symbol		<none></none>	•	
	Signal Integrity		<none></none>	•	
	Boundary Scan		<none></none>	-	

Figure: Design and verification tool selection

### Figure: Select the target device EP4CE55F23C8

# 4.1 Code Editing Input and System Compilation

### 4.1.3 Constraint Item Setting

Assignments →Settings → More Settings

Assignments →Device

e Edit View P	Project 🛛 🎤 Settin	ngs - CNT	10						23
) 🧉 🖬 🎒 🗌	X Di Catacor				ſ	More Analysis & Synthesis Settir	ngs		23
pject Navigator	Categor	y.							
Resources Record	Ger	neral		Analysis	& Synth	Specify the settings for the logic options i or entity in the Assignment Editor will over	in your project. Assignm	ents made to an i	ndividual node
Cyclone IV E: EP40	CESSE23C Lib	raries		Specify o	ptions for		inde die opdon betangs		·
abd CNT 10 A	4 Op	erating Set	tings and Conditions	affect VQ	M or EDIF	Existing option settings:			
UNITO -		Voltage	all contracts and	Ontimiz	nation Tech				
		Temperat	ure	opumz	adon rea	Name:		Setting:	
	A Cor	mpilation Pr	ocess Settings	Spe	eed	Allow Any RAM Size For Recognition		Off	
		Early Timin	ng Estimate	Bal     Bal	anced	Allow Any ROM Size For Recognition		Off	
III .		Physical St	wothesis Optimization			Allow Any Shift Register Size For Reco	gnition	Off	
Hierarchy	Files A ED.	A Tool Setti	ings		:a	Allow Shift Register Merging across Hie	erarchies	Auto	-
		Design En	try/Synthesis	Timin	a Driven C	Allow Synchronous Control Signals		On	
1		Simulation			g-onven a	Analysis & Synthesis Message Level		Medium	
Compilation	-	Formal Ver	rification	V Powe	r-Up Don'	Auto Carry Chains		On	
		Board-Lev	/el	Perfo	rm WYSIV	Auto Clock Enable Replacement		On	
	Ani Ani	alysis & Syn	nthesis Settings			Auto DSP Block Replacement		On	
4 🕨 Compi	ile Design	Verilog HD	Jt Jt Toput	PowerPla	y power d	Auto Gated Clock Conversion		Off	
- P Compa	ine besign	Default Pa	arameters	More Se	ttings	Auto Open-Drain Pins		On	
Device	Figur	re: S	select c	ompila	tior	i synthesis worl	k mode ∞		
Device Select the family a	and device you want	to target f	Select C	ompila	itior	Synthesis Worl	k mode		
Device Select the family a You can install ad	and device you want	to target for rt with the	or compilation. Install Devices comm	OMPIIA		Synthesis worl  Device and Pin Options - CNT1 Category:	k mode		
Device Select the family a You can install add Device family	and device you want iditional device suppo	to target for try with the	SCIECT C	OMPIIA	nenu. able device	Synthesis worl  Device and Pin Options - CNT1  Category: General	k mode	e Pins	
Select the family a You can install ad Device family Family: Cyclor	and device you want iditional device suppo	to target fi	Select C	OMDIIA hand on the Tools n Show in 'Availa Package:	nenu. able devic	Synthesis worl     Device and Pin Options - CNT1     Category:     General     Configuration     Drog reprint Eller	k mode	e Pins	should be used
Select the family i You can install ad Device family Family: Cyclor	and device you want iditional device suppo	to target first with the	Select C	OMDIIA hand on the Tools n Show in 'Availy Package:	nenu. able devic	Synthesis worl     Synthesis worl     General     Configuration     Programming Files     Unused Pins	k mode	s <b>e Pins</b> dual-purpose pins ach pin depend o	s should be used
Device Select the family i You can install ad Device family Family: Cyclor Devices: All	ne IV E	to target for the target for the the	or compilation. Install Devices comm	OMPIIA hand on the Tools n Show in 'Avail Package: Pin count:	nenu. able device FBGA 484	Synthesis worl  Category:  General Configuration Programming Files Unused Pins Dual-Purpose Pins	k mode	e Pins dual-purpose pins ach pin depend o ive Serial	s should be used in the current co
Select the family You can install ad Device family Family: Cyclor Devices: All	and device you want diditional device suppo	to target for the	Select c	and on the Tools m Show in 'Availa Package: Pin count: Speed grade:	nenu. able device FBGA 484 8	Synthesis worl     Synthesis worl     Category:     General     Configuration     Programming Files     Unused Pins     Dual-Purpose Pins     Capacitive Loading	k mode	e Pins dual-purpose pins ach pin depend o ve Serial rdCopy, these se	should be used on the current co ttings apply to th
Select the family i You can install ad Device family Family: Cyclor Devices: All Target device	ne IV E	to target for the	Select c	And on the Tools n Show in 'Availa' Package: Pin count: Speed grade:	nenu. able device FBGA 484 8	Synthesis worl     Synthesis worl     Category:     General     Configuration     Programming Files     Unused Pins     Dual-Purpose Pins     Capacitive Loading     Based Trace Model	k mode	e Pins dual-purpose pins ach pin depend d ive Serial dCopy, these see pins:	should be used in the current co ttings apply to th
Select the family i You can install ad Device family Family: Cyclor Devices: All Target device O Auto device	nd device you want ditional device suppo	re: S	Select c	And on the Tools in Show in 'Availy Package: Pin count: Speed grade: Name filter:	nenu. able device FBGA 484 8	Synthesis worl  Category:  General Configuration Programming Files Unused Pins Dual-Purpose Pins Capacitive Loading Board Trace Model I/O Timing Voltimes	k mode	e Pins Jual-purpose pins ach pin depend o ive Serial dCopy, these se pins:	should be used in the current co ttings apply to th
Select the family i You can install ad Device family Family: Cyclon Devices: All Target device O Auto device O Specific dev	rigur and device you want ditional device suppo ne IV E	re: C	Select c	And on the Tools In Show in 'Availe Package: Pin count: Speed grade: Name filter: Show advi	nenu. able device FBGA 484 8 anced dev	Synthesis worl  Category:  General Configuration Programming Files Unused Pins Dual-Purpose Pins Capacitive Loading Board Trace Model I/O Timing Voltage Pin Placement	k mode	e Pins Jual-purpose pins ach pin depend o ve Serial dCopy, these se pins: me	should be used on the current co ttings apply to th
Select the family i You can install ad Device family Family: Cyclor Devices: All Target device Auto device Specific device	and device you want iditional device suppo ne IV E II e selected by the Fitt vice selected in 'Availa	re: S to target fi rt with the re: able device	s' list	ompila hand on the Tools n Show in 'Availa Package: Pin count: Speed grade: Name filter: Show adv	nenu. able devic FBGA 484 8 anced dev	Synthesis worl	k mode	ce Pins dual-purpose pins ach pin depend o ve Serial d/Copy, these se pins: me Usi	; should be used in the current co ttings apply to th e as programmin
Select the family . You can install ad Device family Family: Cyclor Devices: All Target device Auto device Specific dev Other: n/a	I and device you want didtional device support ine IV E iii e selected by the Fitth vice selected in 'Availate a	re: 2	s' list	And on the Tools in Show in 'Availat Package: Pin count: Speed grade: Name filter: Show adv. Device and Pin.	nenu. able devic FBGA 484 8 anced dev Options	Synthesis worl	K mode Specify how of Specify how of which is: Act Note: For Har Dual-purpose Na DCLK Data[0]	e Pins Jual-purpose pins ach pin depend o ve Serial rdCopy, these se pins: me Us Us	should be used in the current co ttings apply to th e as programmin input tri-stated
Select the family i You can install ad Device family Family: Cydor Devices: All Target device ③ Auto device ③ Specific dev ③ Other: n/a	HIGUI and device you want ditional device suppo ne IV E II e selected by the Fitt vice selected in 'Availa	re: 2	s' list	And on the Tools in Show in 'Availy Package: Pin count: Speed grade: Name filter: Show adv. Device and Pin	nenu. able devic FBGA 434 8 anced dev Options.	Synthesis worl	k mode	e Pins Jual-purpose pins ach pin depend o ive Serial dCopy, these see pins: me Uss As O As	should be used in the current co ttings apply to th e as programmin input tri-stated input tri-stated
Select the family i You can install ad Device family Family: Cyclor Devices: All Target device Auto device Specific dev Other: n/a Available devices:	e selected by the Fitty is selected in 'Availa's	re: S to target f rt with the er able device:	s' list	And on the Tools of Show in 'Availa' Package: Pin count: Speed grade: Name filter: Show adva Device and Pin	nenu. able devic FBGA 484 8 anced dev Options	Synthesis worl	k mode	te Pins dual-purpose pins ach pin depend o ve Serial dCopy, these se pins: me Usi As 0 As 0 As	should be used in the current co ttings apply to the e as programmin input tri-stated e as regular I/O
Select the family i You can install ad Device family Family: Cyclor Devices: Al Target device Auto device Specific dev Other: n/a Available devices: Name	rigur and device you want iditional device suppo ne IV E e selected by the Fitte vice selected in 'Availa a core Voltage	to target fr tr with the able devices	Select c	And on the Tools n Show in 'Availa' Package: Pin count: Speed grade: Name filter: Show adv. Device and Pin Memory Bits	nenu. able devic FBGA 484 8 anced dev Options Eml	Synthesis worl	K mode Specify how of Specify how of Specify how of Specify how of Specify how of Specify how of Specify how of Which is: Act Note: For Har Dual-purpose Na DCLK Data[1]/ASD Data[1]/ASD Data[1]/ASD Data[1]/ASD	te Pins dual-purpose pins ach pin depend o ve Serial rdCopy, these se pins: me Usi Usi Co As O As O As O As O As	should be used in the current co titings apply to t e as programmin input tri-stated input tri-stated as regular I/O input tri-stated
Select the family i You can install ad Device family Family: Cyclor Devices: Al Target device O Auto device O Specific dev O Other: n/a Available devices: Name EP4CE15F23C8	re IV E e selected by the Fitty vice selected in 'Availar core Voltage 1.2V	to target first with the term able devices the ser able devices 15408	s' list	And on the Tools in Show in 'Availy Package: Pin count: Speed grade: Name filter: Speed grade: Name filter: Show adv. Device and Pin Memory Bits 516096	nenu. able device FBGA 484 8 anced dev Options Em 112	Synthesis worl	K mode	e Pins Jual-purpose pins ach pin depend o ve Serial dCopy, these se pins: me Usi As O As Usi Usi Usi CO As Parallel pins Usi	should be used in the current co ttings apply to t e as programmin input tri-stated e as regular I/O input tri-stated e as regular I/O
Select the family i You can install ad Device family Family: Cyclor Devices: Al Target device Auto device Other: n/a Available devices: Name EP4CE15F23C8 EP4CE30F23C8	e selected by the Fitte Core Voltage 1.2V 1.2V	to target firt with the ter able devices 15408 28848	s' list	And on the Tools of Show in 'Availd Package: Pin count: Speed grade: Name filter: Speed grade: Name filter: Speed grade: Name filter: Device and Pin Memory Bits 516096 608256	nenu. able devic FBGA 484 8 anced dev Options Em 112 132	Synthesis worl	K mode	e Pins Jual-purpose pina do pin depend o tve Serial dCopy, these se pins: me Usi ncso As Parallel pins Usi Usi	should be used on the current co titings apply to t input tri-stated input tri-stated e as regular I/O e as regular I/O e as regular I/O

Figure: Select the target device and operation mode

(1) Select compilation constraints. (2) choose the way to configure the device. (3) choose configuration device and programming mode. (4) select the target device pin port state.

## 4.1 Code Editing Input and System Compilation

### 4.1.4 Synthesis and Compilation

Processing -> Start Compilation

Project Navigator       Image: Completion Report - CNT 10         Entity       Logic Cells       d Logic F       I/O Report - CNT 10         Cyclone IV E:       EP4CESSF23C8       Image: CNT 10				
Task     Assembler     TimeQuest Timing Analyzer     Total registers     4       Image: Compile Design     OC     Image: TimeQuest Timing Analyzer     Image: Total pins     13 / 325 (4 %)       Image: Compile Design     OC     Image: Compile Design     Image: Compile Design     Image: Compile Design       Image: Compile Design     OC     Image: Compile Design     Image: Compile Design     Image: Compile Design       Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design       Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design       Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design       Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design       Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design       Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design       Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design     Image: Compile Design       Image: Compile Design     Image: Compi	Project Navigator I 6 X Entity Logic Cells d Logic F I/O Re Cydone IV E: EP4CE55F23C8 CVT 10 1 2 9 (9) 4 (4) 0 (0) Hierarchy Files Pesign Units IP Hierarchy Files Pesign Units IP Tasks IP Tosks IP Compilation Customize	Home       Fable of Contents     Flow S       Flow Summary     Flow S       Flow Settings     Flow Settings       Flow Non-Default Global Sett     Top-le       Flow Clapsed Time     Flow Log       Flow Log     Total le       Flow Settings     Total le       Flow Log     Total le       Fitter     To	Summary Status tus II 64-Bit Version sion Name evel Entity Name y ce g Models logic elements Total combinational functions Dedicated logic registers	Compilation Report - CNT10 Successful - Tue May 23 10:36:07 2017 13.1.0 Build 162 10/23/2013 SJ Full Version CNT10 CNT10 Cydone IV E EP4CE55F23C8 Final 9 / 55,856 ( < 1 % ) 9 / 55,856 ( < 1 % ) 4 / 55,856 ( < 1 % )
	Task     Image: Compile Design     OC       Image: Compile Design	Assembler     Total r     Total r	registers pins virtual pins memory bits edded Multiplier 9-bit elements PLLs	4 13/325(4%) 0 0/2,396,160(0%) 0/308(0%) 0/4(0%)

Figure: Report information after the entire compilation is error-free Compilation includes Quartus II's multiple processing operations on the design input, including input file troubleshooting, netlist file extraction, logic synthesis, adaptation, and assembly files (simulation files and programming profile) generation, and timing analysis of the project.

## 4.1 Code Editing Input and System Compilation

### 4.1.5 Application of RTL Viewer



Select the Tools  $\rightarrow$  Netlist Viewers



### If using Modelsim:

Options	23
	22. CS

#### Category:

/ General	EDA Tool Options		
EDA Tool Options Fonts	Specify the location	of the tool executable for each third-party EDA tool:	
Headers & Footers Settings	EDA Tool	Location of Executable	
Notifications	Precision Synthesis		
Libraries	Synplify		
License Setup Preferred Text Editor	Synplify Pro		
Processing	Active-HDL		
Tooltip Settings	Riviera-PRO		
Colors	ModelSim		
Fonts	QuestaSim		
	ModelSim-Altera	E:\altera\13.1\modelsim_ase\win32aloem	

Figure: Viewing the Quartus Simulation Tool Path to Modelsim Simulation Software

Make sure the simulation tool in Quartus II points to the path where Modelsim is located



### (1) Open the Simulation Waveform Editor

	New Quartus II Project	
4	Design Files	
	AHDL File	
	Block Diagram/Schematic File	
	EDIF File	
	Qsys System File	
	State Machine File	
	SystemVerilog HDL File	
	Td Script File	
	Verilog HDL File	
	VHDL File	
ð	Memory Files	=
	Hexadecimal (Intel-Format) File	
	Memory Initialization File	
đ	Verification/Debugging Files	
	In-System Sources and Probes File	
	Logic Analyzer Interface File	
	SignalTap II Logic Analyzer File	
	Liniversity Program VWE	

File Edit View	Simulati	on Heli	ף <b>ג</b> (H ₩X	) \c	<u>X</u>	2 )(B		Ð j	in an	2	1	0	<b>#</b>	門	é		
Master Tim <mark>e</mark> Bar: 0	ps		•	•	Pointe	er: 38	87.6	ns			Ì	In	ter	val		387	.6 r
Name	alue a 0 ps	0 ps D ps		160.	0 ns		3	20.	0 n:	s				48	30.(	) ns	5

CNT10 varef

File->New->Vector Waveform File-> Zoom ->Fit in Window



### (2) Set the simulation time

Simulation Wave	form Editor - D:/MY_PROJECT/CNT10 - CNT10 - [CNT10.vwf]
- K. C.	九 🍊 江 泊 聯 次 返 次 池 🗟 式 🍋 🐻 晄
Master Time Bar: 0 p	Pointer: 97.0 ns Interval: 97.0
Name	Value at 0 ps 5.12 us 10.24 us 15.36 us 20.48 us 25.6 0 ps
	S End Time
	Set End Time
	End Time: 55.0
	OK Cancel

Figure: Set the simulation time

Edit-> Set End Time (usually 10~100 us)



### Use Node Finder to select the signal nodes into the waveform

View Project Assigne	ents Processing Icol	s Mindow Help	
Utility Windows		Y Project Mavigato	or Alt+0
Enll Seran	C++1+11++S=+++	Node Einder	A1 (+1
a run ocreen	CULTARCOPACE	🚺 Icl Console	A1 1+2
Eit in Window	Ctrl+¥	E Hessages	A1 1+3
C Zoom In	Ctrl+Space	E Status	A1 1+4
Q Zoom Qut	Ctrl+Shift+Space	E Change Manager	A1 1+5
Q Zoon		Tasks	A1 1+6

Bode Tinder Master Time Bac Named 1 · Filter, Pins: all Customize. List Look in MULTER Include subentities 23 Nodes Found Name Creator Type ٠ A **1**20 CA. Input Group User entered 0 5 3 Unassigned D A[1] User entered Unaccigned Input. 210 1 2 A121 User entered Unassigned Input ALC: User entered Unassigned Input (A44) Unassigned Input Uper entered **€**₽8 User entered Unattioned Input Group B(1) Unassigned Input User enileted B[2] User entered Unassigned Input DE18 40 Unassigned Incut User entered

Figure: Open Signal Node Query Window

Figure: Drag the signal node into the waveform editor

If the node name is not displayed, compile once again, and the signal nodes will be shown.



### Join signal nodes needed for simulation

Value at 0 ps 80.0 ns 160.0 ns 240.0 ns   0 ps Insert Node or Bus X     Name: X     Name: Name:     Name: OK   Type: INPUT   Cancel Value type:   9-Level Node Finder   Node Finder Node Finder   Node Finder Node Finder     Name: Input     Name: Cancel   Value type: 9-Level   Node Finder Node Finder   Node Finder Input Group   DATA Input Group   DATA[0] Input	OK Cance
U ps       Insert Node or Bus       Image: Color and the second s	Cance
Name:     OK       Type:     INPUT       Value type:     9-Level       Radix:     Binary         Node Finder         Node Finder        Node Finder         Node Finder         Node Finder         Node Finder         Node Finder         Node Finder         Node Finder             Node Finder         Node Finder	
Name:     OK     Name     Type       Type:     INPUT     Cancel       Value type:     9-Level       Radix:     Binary         Node Finder         Name     Type       Input         Name     Type       Input         Name     Type       Input         Name     Type       Input         Name     Type         Name     Type         Name             Name         Name            Node Finder         Node Finder         Node Finder         Node Finder         Name         Name	
Type:       INPUT       Cancel       in       CLK       Input         Value type:       9-Level       Node Finder       Node Finder       Output       Output         Radix:       Binary       Node Finder       Input       Input       Input       Output         Input       DATA       Input       Input       Input       Input       Input	
Value type:     9-Level     Image: Second Se	
Radix:     Binary     Node Finder     Image: Data     Input Group     Data     Data     Imput Group       Image: Data     Image: Data     Imput Group     Imput Group     Imput Group     Imput Group     Imput Group	
DATA[0] Input	
Bus width: 1 DATA[1] Input	
Start index: 0 DATA[2] Input	
Display gray code count as binary count	
DOUT Output Group	

Figure: Join signal nodes needed for simulation

### Radix -> Hexadecimal



Setting the bus data format

Sin	nulation V	Vaveform B	ditor - D:/MY_PRO	DJECT/CNT10 - CNT10 - [CNT10.vwf]*
ile	Edit Viev	v Simulatio	n Help 💎	
(b)	1	관 <u>▲</u> ヱ	XI XH W XC X	@ X2 XB 式 式 🚈 🗐 联
Maste	r Time Bar:	0 ps		Pointer: 131.42 ns Interval: 131.42 ns
	12811111	Value at	0 ps 5.12 us	Node Properties 23 30.72 us
	Name	0 ps	0 ps	Name: DOUT OK
in_	CLK	BO		Type: OUTPUT
<b>i</b>	DATA	но		Value type: 9-Level
İn	EN	во		Radix: Hexadecimal
in_	LOAD	во		Bus width: 4
in_	RST	B 0		Display gray code count as binary count
out	COUT	вх		
방		B XXXX		XXXX

### Figure: Setting the bus data format

			-						
		Value at	0 ps	5.12 us	10.24 us	15.36 us	20. <mark>4</mark> 8 us	25.6 us	30
	Name	0 ps	0 ps	(	🚱 Clock		23	J	
in_	CLK	в 0	J	WW	Base waveform	on time period	J	] MMM	ЛЛ
is.	▷ DATA	но			Period: 900.0	)	ns 🔻	0	
in_	EN	В 0			Offset: 0.0		ns 🔻		
in 🕒	LOAD	BO			Duty cycle (%)	: 50			
in D	RST	В 0							
out	COUT	вх				OK	Cancel		$\sim$
액	▶ DOUT	нх			1 1 1 1	1 1 1	1 1 1 1	X	

## Setting the clock parameters

### Figure: Setting clock parameters





### Figure: Editing the excitation waveform





### 4.3.1 Pin Assignment



Figure: Experimental Circuit for FPGA in Mode 0

Experimental Circuit for FPGA



### 4.3.1 Pin Assignment

	I Categ	All Locations PLL Comb. cell			
	치 지 지	Information: This cell sp Edit:	ecifies the entity o	r node you want to assi	gn to the location specified in the L
100 EM		То	Location	Enabled	
111	1		Node Finde	r	
8			Select Ass	ignment Group	]

Figure: Locking the pin of the FPGA by using the Assignment Editor

Assignments->Assignment Editor->Locations or PIN planner

To: the port in the program Location: the pin on the board, such as PIN\_23



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	Node Name	Direction	Locatio
	Input				PIN_J4	in_ CLK	Input	PIN_AB6
STOOL COUT	Output				PIN_T8	COUT	Output	PIN_AA1
In_ DATA[3]	Input				PIN_R8	DATA[3]	Input	PIN_AB5
In_ DATA[2]	Input				PIN_R10	DATA[2]	Input	PIN_AA3
In_ DATA[1]	Input				PIN_T9	DATA[1]	Input	PIN_W2
In_ DATA[0]	Input				PIN_V6	DATA[0]	Input	PIN_U2
DOUT[3]	Output				PIN_R9	OUT DOUT[3]	Output	PIN_V2
DOUT[2]	Output				PIN_T5	OUT DOUT[2]	Output	PIN W1
STOUT[1]	Output				PIN_R6	OUT DOUT[1]	Output	PIN R2
STLOOUT[0]	Output				PIN_P8	OUT DOUT[0]	Output	PIN U1
in_ EN	Input				PIN_T7	in_ EN	Input	PIN Y7
ID_ LOAD	Input				PIN_R7	LOAD	Input	PIN AA6
In_ RST	Input				PIN_P4	B_ RST	Input	PIN_AB3

Figure: The newly opened Pin Planner window

Figure: After pin locking is completed

After locking the PIN, you must compile the project again, Start Compilation



### 4.3.2 Compiled File Download

Edit View	Processing Tools Window	Help SV										
, Hardware Setup Enabl <mark>e real-tim</mark> e I	SP to allow background progra	USB-Blaster [USB-0] to allow background programming (for MAX II and MAX V devices)									Mode:	
Start Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
Stop	output_files/CNT10.sof	EP4CE55F23	002B571D	002B571D								
uto Detect												
Delete												
Add File												
hange File	TDI											
Save File												
Add Device	EP4CE55	F23										

Figure: Select JTAG programming mode to configure SOF file into FPGA

Download SOF configuration file into FPGA. Install the driver and find the hardware device.



elect a programming h	ardware setup to	use when prog	ramming devices	. This programming		
araware setup applies		ant programmer	THE WORK			
urrently selected hard	dware: USB-Bla	USB-Blaster [USB-0]				
Available hardware it	ems					

Figure: Add a programming download method



### 4.3.4 USB-Blaster Driver Installation

- One end of the USB Blaster programmer into the USB port of the PC. A USB driver dialog box will pop up.
- Select the user to search for the driver according to the dialog guidance.
- It is assumed that the Quartus II software is installed on the E drive and the driver's path is E:\altera\quartus\drivers\usb-blaster.

 $D:\latera\quartus 90\drivers\use-blaster$ 



### 4.4.1 Half-adder Design



Figure: Circuit structure of a half-adder

A	в	so	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure: Truth table of half adder



Figure :Simulation function

$$SO=A \oplus B; CO=A \cdot B$$



X	Cut	Ctrl+X			
h	Copy	Ctrl+C			
R	Paste	Ctrl+V	2		
×	Delete	Del			
D!	Update Symbol o	or Bloc <u>k</u>			
	<u>Z</u> oom		۲		
	Show		۲		
	<u>I</u> nsert		•	Symbol	j
	Open Symbol Fil	Le		Symbol as Block <u>.</u>	
	Open AHDL Inclu	ıde File			

Libraries:	
A C d:/altera/13.1/quartus/libraries/	
P megafunctions	
D Chathers	
D primitives	
and the second se	
*	N
Nama	pin_name1
Name;	
input	•
Repeat-insert mode	
Insert symbol as block	
Launch Mena-Wizard Plug-In	
Launch hicga wizara hiug-th	

Figure: Select Open Component Entry Window

Figure: Input Pins in the Component Input Dialog Box



🐇 Quartus II - D:/ADDER/h_adder	h_adder = [h_adder.bdf]
File       Edit       Yiew       Project       Assignments         Pro       Dpen       Ctrl+N         Glose       Ctrl+F4         Open Project       Mizard         Open Project       Ctrl+J         Convert       MAX+PLUS II Project         Save       Ctrl+S         Save       Ctrl+S         Save As       Save Current Report Section As         File       File	rocessing Tools Window Help h_adder h_adder.bdf A INPUT NCC B INPUT A NCC A NCC INPUT SO OUTPUT SO OUTPUT CO inst OUTPUT CO
— Create / Update 🕨 🕨	Create HDL Design File for Current File
Export	Create <u>Symbol Files for Current File</u>
Convert Programming Files	Create AHDL Include Files for Current File

Figure: Complete design and pack the half adder as a component for calling in higher level design



23

## 4.4 Circuit Schematic Design Flow

### 4.4.2 Top-level Design of Full-adder

what is the wo	rking director	v for this project?				
D: ADDER						
What is the na	me of this pro	iect?				
f_adder						
What is the na exactly match	me of the top he entity nam	level design entity e in the design file	for this proj	ect? This name i	s case sensi	ive and must
1 alles						

Figure: Full adder f\_adder.bdf project settings

Figure: Add a half adder to the f adder project

h adde

B CO

SO



🚼 Symbol

Libraries: Project h\_adder C d:/altera/13.1/quartus/libraries/ megafunctions mosfunctions C others primitives b b others

Name: h adder 🔺 🗁 logic

D and 12

₽ and2

...

Figure: Full adder f\_adder circuit diagram



### 4.4.3 Timing Simulation and Hardware Testing of Full Adders



Figure: Simulation waveform of the full adder



## 4.5 Pin Assignment Using Attributes

Direct control of pin locking in Verilog code

### [Example]

. . .

module CNT10 (CLK,RST,EN,LOAD,COUT,DOUT,DATA); input [3:0] DATA /\* synthesis chip\_pin="AB5,AA3,W2,U2" \*/; output [3:0] DOUT /\* synthesis chip\_pin="V2,W1,R2,U1" \*/; output COUT /\* synthesis chip\_pin="AA1" \*/; input CLK /\* synthesis chip\_pin = "AB6" \*/; input EN /\* synthesis chip\_pin = "Y7" \*/; input RST /\* synthesis chip\_pin = "AB3" \*/; input LOAD /\* synthesis chip\_pin = "AA6" \*/;

- (1) It must correspond to the determined target device, and the attribute statements in this book apply only to Quartus II;
- (2) It can only be defined in the top-level design file.